IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A semiconductor device having a function verification capability comprising:

an internal verification block receiving and then storing a desired first input value and a desired cycle value being a timing to supply the first input value to a target verification block corresponding to the internal verification block, both values being for use in an operation verification according to execution of internal verification instructions being executed in synchronization with one stage in pipeline for the semiconductor device during the operation verification, and supplying the first input data to the target verification block instead of a second input data being for use in a normal operation after a time indicated by the cycle time is elapsed after receiving and storing the first input data and the cycle value.

2. (Original) The semiconductor device having a function verification capability according to claim 1, wherein a plurality of the first input data and the corresponding cycle values are set to the internal verification block continuously, and each of the first input data is supplied to the target verification block every a lapse of the corresponding cycle value.

3. (Original) The semiconductor device having a function verification capability according to claim 1, wherein the internal verification block comprises:

a register storing the first input value;

a counter, to which the cycle value is set, decrementing this cycle value;

a detector detecting that the value of the counter becomes zero; and

a multiplexer selecting the first input data stored in the register instead of the second input data for use in the normal operation when the detector detects that the value of the counter becomes zero, and supplying the selected one to the target verification block.

4. (Original) The semiconductor device having a function verification capability according to claim 1, wherein the internal verification block comprises:

a data register file storing a plurality of the continuous first input data;

a wait register file storing a plurality of the cycle values corresponding to a plurality of the first input data;

an address pointer supplying a writing address and a reading address to the data register file and the wait register file;

a counter decrementing the cycle value set in the wait register file;

a register storing the first input data read from the data register file in synchronization with the operation of the counter;

a detector detecting that the value of the counter becomes zero; and

a multiplexer selecting the first input data stored in the register instead of the second input data for use in the normal operation when the detector detects that the value of the counter becomes zero, and supplying the selected one to the target verification block.

5. (Original) The semiconductor device having a function verification capability according to claim 1, wherein the internal verification instructions are described in a verification program to verify the operation of the target verification block and executed in synchronization with pipeline operation.

6. (Original) The semiconductor device having a function verification capability according to claim 2, wherein the internal verification instructions are described in a verification program to verify the operation of the target verification block and executed in synchronization with a pipeline operation.

7. (Original) The semiconductor device having a function verification capability according to claim 3, wherein the register, the counter, the detector, and the multiplexer forming the internal verification block operate in synchronization with a pipeline operation.

8. (Original) The semiconductor device having a function verification capability according to claim 4, wherein the data register file, the wait register file, the address pointer, the counter, the register, the detector, and the multiplexer forming the internal verification block operate in synchronization with a pipeline operation.

9. (Original) The semiconductor device having a function verification capability according to claim 1 comprises a plurality of the internal verification blocks and the target verification blocks, and each internal verification block corresponds to each target verification block in a one-to-one correspondence between them.

10. (Original) The semiconductor device having a function verification capability according to claim 2 comprises a plurality of the internal verification blocks and the target verification blocks, and each internal verification block corresponds to each target verification block in a one-to-one correspondence between them.

11. (New) A semiconductor device having a function verification capability comprising:

an internal verification block receiving and then storing a first input value and a cycle value being a timing to supply the first input value to a target verification block corresponding to the internal verification block, both values being for use in an operation verification according to execution of internal verification instructions during the operation verification, and supplying the first input data to the target verification block instead of a second input data being for use in a normal operation after a time indicated by the cycle time is elapsed after receiving and storing the first input data and the cycle value,

wherein, the internal verification block comprises:

a data register file storing a plurality of the continuous first input data;

a wait register file storing a plurality of the cycle values corresponding to a plurality of the first input data;

an address pointer supplying a writing address and a reading address to the data register file and the wait register file;

a counter decrementing the cycle value set in the wait register file;

a register storing the first input data read from the data register file in synchronization with the operation of the counter;

a detector detecting that the value of the counter becomes zero; and

a multiplexer selecting the first input data stored in the register instead of the second input data for use in the normal operation when the detector detects that the value of the counter becomes zero, and supplying the selected one to the target verification block.

12. (New) A semiconductor device having a function verification capability according to claim 11, wherein the data register file, the wait register file, the address

pointer, the counter, the register, the detector, and the multiplexer forming the internal verification block operate in synchronization with a pipeline operation.